UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/611,395	06/30/2003	Shriram Ramanathan	42P16666	1525

8791 7590 06/22/2006

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
DOTY, HEATHER ANNE	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 06/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/611,395	RAMANATHAN ET AL.	
	Examiner	Art Unit	
	Heather A. Doty	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 13-26* is/are rejected.

7)☒ Claim(s) *12 and 27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless – (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-6 and 13-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Tong et al. (U.S. 2004/0157407).

Regarding claim 1, Tong et al. teaches a method comprising:

- depositing a layer of metal on each of a number of conductors disposed on a first wafer (paragraphs 0048, 0075-0076);
- aligning the first wafer with a second wafer, the second wafer having a number of conductors disposed on a surface thereof (Fig. 2b);
- physically contacting the metal layer on each of the conductors of the first wafer with a mating one of the conductors on the second wafer (Fig. 2b); and
- forming a bond between the metal layer on each of the conductors of the first wafer and the mating one conductor of the second wafer (paragraph 0051; Fig. 2c), wherein regions of the first and second wafer surfaces surrounding the mating conductors remain unbonded (Fig. 2c shows regions on the left and right sides of the wafers unbonded; paragraph

0051 discloses that an unbonded region with a width W remains, despite efforts to minimize W).

Regarding claim 2, Tong et al. teaches the method of claim 1, and further teaches, prior to depositing the metal layer on each of the conductors of the first wafer, removing dielectric material from the surface of the first wafer (paragraph 0063).

Regarding claim 3, Tong et al. teaches the method of claim 1, and further teaches, prior to depositing the metal layer on each of the conductors of the first wafer, removing native oxide from the conductors (paragraph 0075).

Regarding claims 4 and 5, Tong et al. teaches the method of claim 1, and further teaches that the conductors of the first wafer comprise copper and the metal comprises gold, platinum, or palladium (paragraphs 0075-0077).

Regarding claim 6, Tong et al. teaches the method of claim 1, and further teaches that the bond is formed at a temperature between approximately 100 and 300 degrees Celcius (paragraph 0060 discloses annealing within the claimed temperature range to strengthen the room-temperature bond).

Regarding claim 13, Tong et al. teaches a method comprising:

- depositing a layer of a first metal on each of a number of conductors disposed on a first wafer (paragraphs 0048, 0075-0076);
- depositing a layer of a second metal on each of a number of conductors disposed on a second wafer (paragraphs 0048, 0075-0076);
- aligning the first wafer with the second wafer (Fig. 2b);

- physically contacting the metal layer on each of the conductors of the first wafer with the metal layer on a mating one of the conductors of the second wafer (Fig. 2b); and
- forming a bond between the metal layer on each of the conductors of the first wafer and the metal layer on the mating one conductor of the second wafer (paragraph 0051; Fig. 2c), wherein regions of the first and second wafer surfaces surrounding the mating conductors remain unbonded (Fig. 2c shows regions on the left and right sides of the wafers unbonded; paragraph 0051 discloses that an unbonded region with a width W remains, despite efforts to minimize W).

Regarding claim 14, Tong et al. teaches the method of claim 13, and further teaches, prior to depositing the metal layer on each of the conductors of the first wafer, removing dielectric material from the surface of the first wafer (paragraph 0063).

Regarding claim 15, Tong et al. teaches the method of claim 13, and further teaches, prior to depositing the metal layer on each of the conductors of the first wafer, removing native oxide from the conductors (paragraph 0075).

Regarding claims 16-18 and 20, Tong et al. teaches the method of claim 13, and further teaches that the conductors of each of the first and second wafers comprise the same metal, wherein that metal is copper, and wherein each of the first and second metals comprises gold, platinum, or palladium (paragraphs 0047-0050 discloses giving both wafers the same pre-bonding treatment; paragraph 0075 discloses copper, gold, and platinum; paragraph 77 discloses palladium).

Regarding claim 21, Tong et al. teaches the method of claim 13, and further teaches that the bond is formed at a temperature between approximately 100 and 300 degrees Celcius (paragraph 0060 discloses annealing within the claimed temperature range to strengthen the room-temperature bond).

Regarding claim 19, Tong et al. teaches the method of claim 13, and further teaches that the first metal and the second metal are different (paragraph 0018 discloses that an advantage to the invention is allowing bonding of different materials on different substrates).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tong et al. (U.S. 2004/0157407) in view of Wolf et al. (Silicon Processing for the VLSI Era, vol. 1, 1986).

Regarding claims 7 and 22, Tong et al. teaches the methods of claims 1 and 13 (note 35 U.S.C. 102(e) rejection above), but is silent regarding the manner in which the layer of metal on each of the conductors of the first wafer is deposited.

Wolf et al. teaches that it is commonplace to use lift-off techniques to pattern metal layers in silicon processing. Such lift-off techniques comprise forming a blanket

layer of the metal on the surface of the conductor and removing portions of the metal layer (pp. 535-536).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the methods taught by Tong et al., and further use lift-off methods to deposit the layer of metal on each of the conductors of the first wafer, comprising forming a blanket layer of the metal over the conductors and the surface of the first wafer and removing the metal from at least portions of the first wafer surface. The motivation for doing so, at the time of the invention, would have been that Wolf et al. teaches that this is a common method for patterning metal in semiconductor processing.

Claims 8-11 and 23-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tong et al. (U.S. 2004/0157407) in view of Neuhaus et al. (U.S. 2002/0027294).

Regarding claims 8-11 and 23-26, Tong et al. teaches the methods of claims 1 and 13 (note 35 U.S.C. 102(e) rejection above), but does not teach that depositing the layer of metal on each of the conductors of the first wafer comprises selectively depositing the metal on each of the conductors, that selectively depositing the metal comprises an electroless plating process, an electroplating process, or a contact displacement plating process, that the metal layer on each of the conductors of the first wafer comprises a number of islands, or that the islands are selectively deposited on each of the conductors of the first wafer.

Neuhaus et al. teaches a method of performing metal-to-metal bonding for semiconductor wafers comprising electroplating a number of metallic islands (particles) to a metallized contact, which is a mode of selective deposition (paragraphs 0027-0028, 0038, and 0073). Neuhaus et al. teaches that this method eliminates several manufacturing steps, which simplifies the process for component assembly. It also provides improved electrical performance, such as lower metal-to-metal contact resistance (paragraph 0021).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the methods taught by Tong et al., and use the method taught by Neuhaus et al. to electroplate metallic islands onto each of the conductors of the first wafer. The motivation for doing so at the time of the invention would have been to eliminate manufacturing steps and to achieve low metal-to-metal contact resistance, as expressly taught by Neuhaus et al.

Response to Arguments

Applicant's primary argument is that as amended, independent claims 1 and 13 recite that regions of the first and second wafer surfaces surrounding the mating conductors remain unbonded, which Tong et al. does not teach (p. 6, paragraph 4). While it is true that Tong et al. teaches that some of the regions of the first and second wafer surfaces surrounding the mating conductors form bonds, other regions do not, such as the regions on the left and right sides of the wafers shown in Fig. 2c. Moreover, Tong et al. discloses in paragraph 0051 the presence of unbonded regions having a width W. Tong et al. further discloses that the width of these regions can be reduced as

long as the thickness of the metal pads is not too large, but the regions nonetheless remain, as shown in Fig. 2c.

Allowable Subject Matter

For reasons indicated in the Office Action dated 6/01/2005, claims 12 and 27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Heather A. Doty, whose telephone number is 571-272-8429. The examiner can normally be reached on M-F, 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

had

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800